UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,769	06/27/2003	Scott A. Hareland	42P15685	6439

7590 08/14/2007

Michael A. Bernadicou
BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
Seventh Floor
12400 Wilshire Boulevard
Los Angeles, CA 90025

EXAMINER	
SUCH, MATTHEW W	

ART UNIT	PAPER NUMBER
2891	

MAIL DATE	DELIVERY MODE
08/14/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/607,769	HARELAND ET AL.	
	Examiner	Art Unit	
	Matthew W. Such	2891	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 July 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 6 is objected to because of the following informalities: the phrase "is formed said top surface" in Lines 3 and 4 of the claim should read "is formed *on* said top surface". Appropriate correction is required.

2. Claim 12 is objected to because of the following informalities: the phrase "is formed said top surface" in Line 4 of the claim should read "is formed *on* said top surface". Appropriate correction is required.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2, 4-8 and 10-12 are rejected under 35 U.S.C. 102(b) as being anticipated by Maegawa ('513).

5. Regarding claim 1, Maegawa teaches a device having a semiconductor body (Element 3) having a top surface opposite a bottom surface formed above an insulating substrate (Elements 1,

2, 5, in combination). The semiconductor body has a pair of laterally opposite sidewalls (Figs. 4, 8, 19, 22, 23, 30, 32, for example). A gate dielectric (Element 5 around 3) is formed on the top surface of the semiconductor body, on at least a portion of the bottom surface of the semiconductor body, and on laterally opposite sidewalls of the semiconductor body. A gate electrode (Element 6) is formed on the gate dielectric, on the top surface of the semiconductor body and adjacent to the gate dielectric on the laterally opposite sidewalls of the semiconductor body and beneath the gate dielectric on the bottom surface of the semiconductor body (Figs. 4, 8, 19, 22, 23, 30, 32, for example). The gate electrode as a top portion (portion of Element 6 above 3, for example) and a bottom portion (portion of Element 6 below 3, for example) wherein the bottom portion laterally undercuts the top portion (see, for example, Fig. 4D wherein the bottom portion of Element 6 laterally undercuts the top portion). A pair of source/drain regions (Elements S and D) are formed in the semiconductor body on opposite sides of the gate electrode.

6. Regarding claim 2, Maegawa teaches that the semiconductor body can be a single crystal silicon film (Col. 1, Lines 24-25; Col. 2, Lines 46-47).

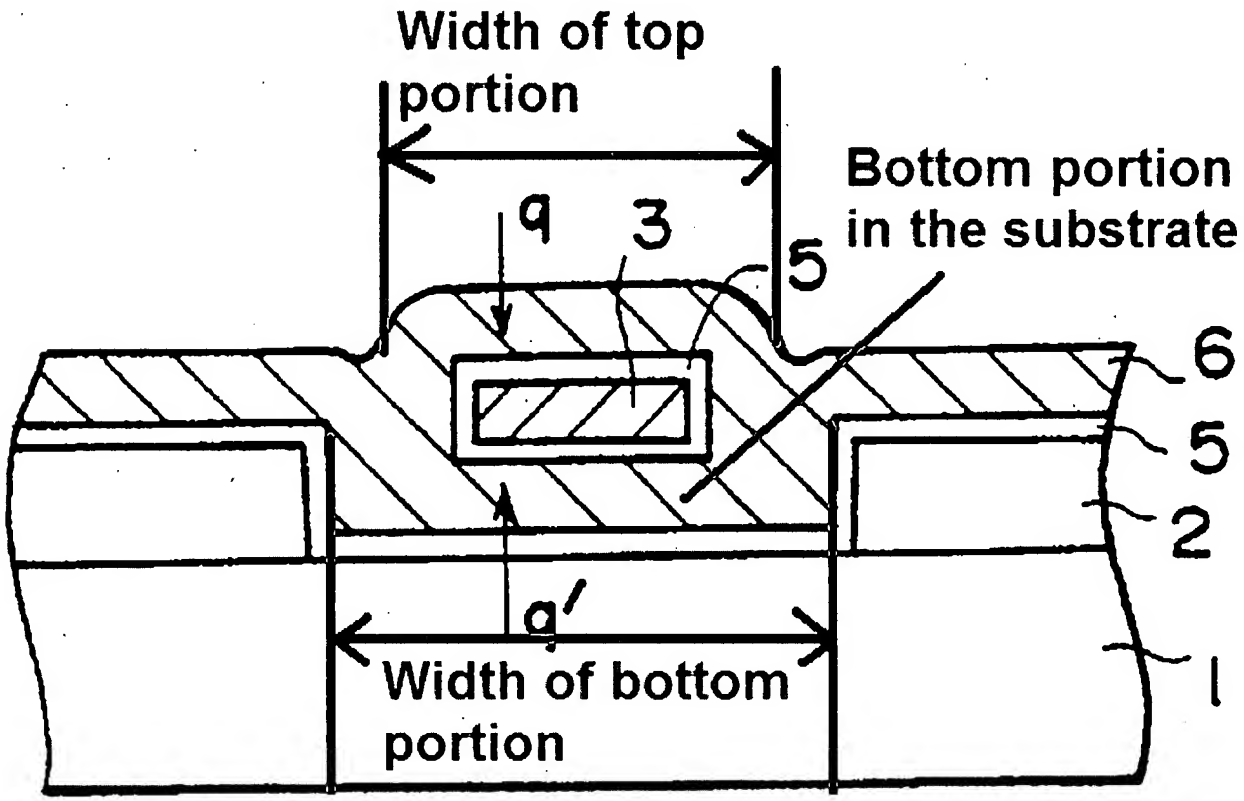
7. Regarding claim 4, Maegawa teaches that the gate electrode is polycrystalline silicon (Element 6, 11, 12; Col. 1, Line 41; Col. 2, Lines 19-20; Col. 6, Line 51).

8. Regarding claim 5, Maegawa teaches that the insulating substrate comprises an oxide film (Elements 2 and 5) on a monocrystalline silicon substrate (Element 1).

9. Regarding claim 6, Maegawa teaches that the device further includes at least one additional semiconductor body (see, for example; Elements 3-1, 3-2, 3-3 in Fig. 19A; Elements 3a, 3b, 3c, 3d, 3e in Fig. 30) having a top surface and a bottom surface, and a pair of laterally opposite sidewalls wherein a gate dielectric layer is formed on the top surface, bottom surface and sidewalls of the at least one additional semiconductor body. The gate electrode is formed on the gate dielectric on the top surface of the at least one additional semiconductor body, and adjacent to the gate dielectric on the laterally opposite sidewalls of the at least one additional semiconductor body, and beneath the gate dielectric on the bottom surface of the at least one additional semiconductor body (Figs. 19A and 30, for example).

10. Regarding claim 7, Maegawa teaches a device having a semiconductor body (Element 3) having a top surface opposite a bottom surface formed above an insulating substrate (Elements 1, 2, 5, in combination). The semiconductor body has a pair of laterally opposite sidewalls (Figs. 4, 8, 19, 22, 23, 30, 32, for example). A gate dielectric (Element 5 around 3) is formed on the top surface of the semiconductor body, on at least a portion of the bottom surface of the semiconductor body, and on laterally opposite sidewalls of the semiconductor body. A gate electrode (Element 6) is formed on the gate dielectric, on the top surface of the semiconductor body and adjacent to the gate dielectric on the laterally opposite sidewalls of the semiconductor body and beneath the gate dielectric on the bottom surface of the semiconductor body (Figs. 4, 8, 19, 22, 23, 30, 32, for example). The gate electrode as a top portion above the insulating substrate (portion of Element 6 above the top plane of Element 2 in Fig. 4D, for example) and a

bottom portion in the insulating substrate (portion of Element 6 below the top plane of Element 2 in Fig. 4D, for example). The bottom portion is wider than the top portion the top portion. A pair of source/drain regions (Elements S and D) are formed in the semiconductor body on opposite sides of the gate electrode.



11. Regarding claim 8, Maegawa teaches that the semiconductor body can be a single crystal silicon film (Col. 1, Lines 24-25; Col. 2, Lines 46-47).

12. Regarding claim 10, Maegawa teaches that the gate electrode is polycrystalline silicon (Element 6, 11, 12; Col. 1, Line 41; Col. 2, Lines 19-20; Col. 6, Line 51).

13. Regarding claim 11, Maegawa teaches that the insulating substrate comprises an oxide film (Elements 2 and 5) on a monocrystalline silicon substrate (Element 1).

14. Regarding claim 12, Maegawa teaches that the device further includes at least one additional semiconductor body (see, for example; Elements 3-1, 3-2, 3-3 in Fig. 19A; Col. 12, Lines 32-35) having a top surface and a bottom surface, and a pair of laterally opposite sidewalls wherein a gate dielectric layer is formed on the top surface, bottom surface and sidewalls of the at least one additional semiconductor body. The gate electrode is formed on the gate dielectric on the top surface of the at least one additional semiconductor body, and adjacent to the gate dielectric on the laterally opposite sidewalls of the at least one additional semiconductor body, and beneath the gate dielectric on the bottom surface of the at least one additional semiconductor body (Figs. 19A and 30, for example).

Claim Rejections - 35 USC § 103

15. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

16. Claims 2 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Maegawa ('513) in view of Yu ('869).

Maegawa teaches the device of claims 1 and 7 wherein the channel material is silicon. Maegawa does not teach other conventional channel materials.

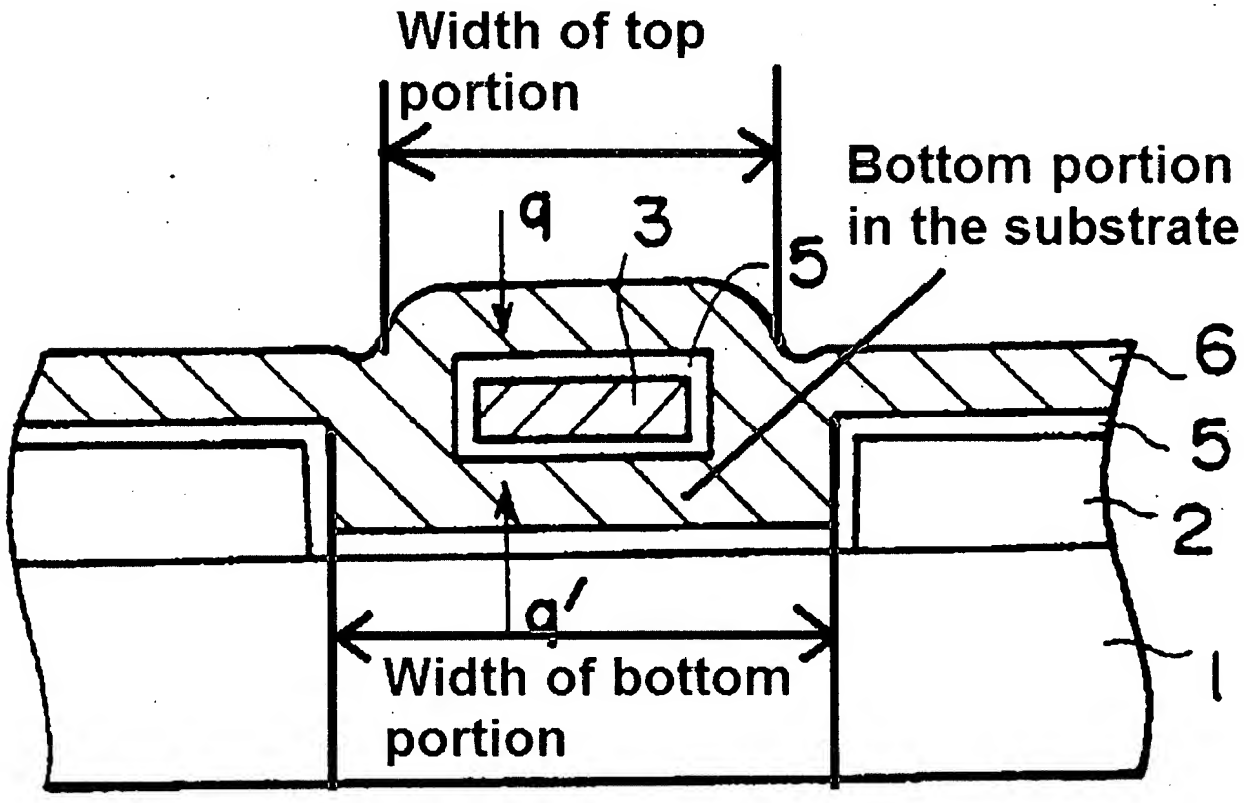
Yu teaches using silicon-germanium as an alternative conventional channel material (Abstract; Col. 3, Lines 1-20) for devices formed on SIO substrates. It would have been obvious to one of ordinary skill in the art at the time the invention was made to use a silicon-germanium channel material as taught by Yu in the device of Maegawa. Yu teaches that germanium inclusion increases the charge carrier mobility of the channel region, producing a faster device (Abstract; Col. 2, Lines 22-31; Col. 4, Lines 65-67).

Response to Arguments

17. Applicant's arguments filed 30 July 2007 have been fully considered but they are not persuasive. The Applicant argues that the prior art of Maegawa does not anticipate the claims.

18. Regarding claims 1-6, the Applicant argues that Maegawa fails to disclose a gate electrode where the bottom portion laterally undercuts the top portion (see Remarks Pages 6-7). In response, the Examiner notes that the manner in which the claim is written does not limit what a "top portion" and a "bottom portion" are defined as. Therefore, the "top portion" can be defined as portion of the gate electrode over the semiconductor body (see, for example, Element 6a above Element 3 in Fig. 8E) and the "bottom portion" can be defined as a portion of the gate electrode under the semiconductor body and undercutting the "top portion" (see, for example, Element 6b undercutting Element 3 and Element 6a in Fig. 8E).

19. Regarding claims 7-12, the Applicant argues that Maegawa fails to disclose a gate electrode that has a top portion above an insulating substrate and a bottom portion formed in the insulating substrate wherein the bottom portion is wider than the top portion (see Remarks Pages 7-8). In response, the Examiner notes that the manner in which the claim is written does not limit what a "top portion" and a "bottom portion" are defined as. Therefore, the "top portion" can be defined as portion of the gate electrode over the semiconductor body (see, for example, Element 6a above Element 3 in Fig. 32E) and the "bottom portion" can be defined as a portion of the gate electrode in the insulating substrate (see, for example, Element 6b in the substrate hole defined by Elements 2 in Figs. 4D and 32E):



Contact Information

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew W. Such whose telephone number is (571) 272-8895. The examiner can normally be reached on Monday - Friday 9AM-5PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bradley W. Baumeister can be reached on (571) 272-1722. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Matthew W. Such
Examiner
Art Unit 2891

MWS
8/7/07

B. WILLIAM BAUMEISTER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800